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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,884	04/21/2004	Bor-Min Tseng	TSM03-0763	5862

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,884	TSENG, BOR-MIN	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 31-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,12,14,15,18,19,31-37 and 40* is/are rejected.

7)☒ Claim(s) *5-8,10,11,13,16,17,38 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

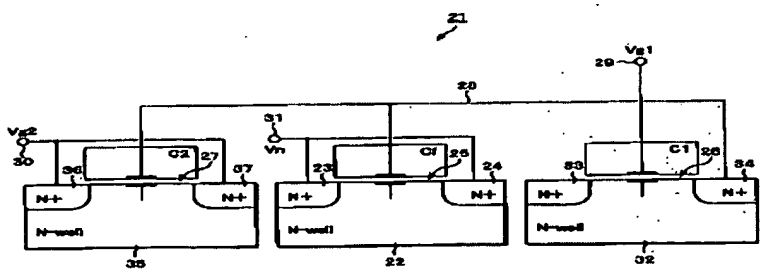
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 9, 12, 14, 15, 18, 31, 33, 34, 35, 37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adan (U.S. Pub. 2003/0136992) in view of Yeo et al. (U.S. Patent 6,521,939).

In re claim 1, **Adan** disclose a method of forming a semiconductor varactor device 21 having improved linearity comprising the steps of:

providing a semiconductor substrate (single silicon substrate) (page 4, paragraph [0055]); forming at least a first and a second differential varactor element on the semiconductor substrate, the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35,**

FIG. 5



forming a first gate **C2** for controlling the first **36** and second **37** N+ doped regions and forming a second gate **Cf** for controlling the second **37** and third **24** N+ doped regions (pages 3-4, paragraphs [0051]-[0053] and FIG. 5);

connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor element to receive power having a the same first voltage **Vg2**; and connecting the first **33**, second **34** and third N+ doped regions of the second differential varactor element to receive power having the same second voltage **Vg1**, the second voltage being different than the first voltage (page 4, paragraphs [0053]-[0055] and FIG. 5).

Adan disclose forming at least a first and a second differential varactor element on the semiconductor substrate wherein the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35** but does not explicitly discloses that the steps of forming first, second and third N+ doped regions in the same N well as recited in independent claim 1.

Yeo, however, discloses a method of forming a semiconductor varactor device comprising the steps of: providing a semiconductor substrate 96; forming a differential varactor element on the semiconductor substrate 96, the forming of the differential varactor elements comprising forming first, second and third N+ doped region 104 in the same N well 100 (col. 5, lines 59-65), forming a first gate 108 for controlling the first and second N+ doped regions 104 and forming a second gate for controlling the second and third N+ doped regions 104 (col. 6, lines 10-42 and FIG. 9).

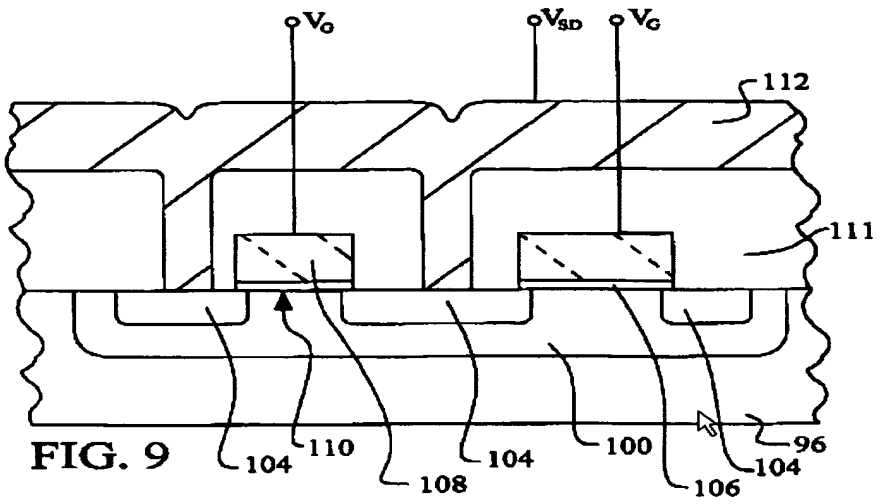


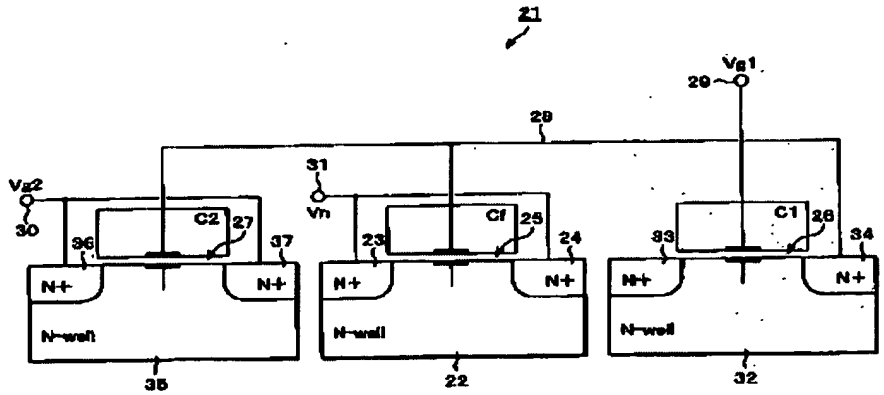
FIG. 9

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Yeo to enable the process of forming the first, second and third N+ doped regions in the same N well of Adan to be performed and furthermore to obtain a high performance varactor on silicon in the manufacture of integrated circuit devices (col. 1, lines 8-11, Yeo).

In re claim 3, as applied to claim 1 above, **Adan** discloses all claimed limitations including the limitation wherein the step of forming the first **C2** and second **Cf** gates comprises the step of forming a first N-type gate and forming a second N-type gate (page 3, paragraph [0052]).

In re claim 9, as applied to claim 1 above, **Adan** discloses all claimed limitations including the limitation connecting the first gate **C2** of the first and second differential varactor elements together at a first terminal **Vg2** and connecting the second gate **Cf** of the first and second differential varactor elements together at a second terminal **Vn** (page 4, paragraph [0055] and FIG. 5)

FIG. 5



In re claim 12, as applied to claim 9 above, **Adan** discloses all claimed limitations including the limitation connecting the first **Vg2** and second **Vg1** terminals to an oscillator circuit as a voltage controlled capacitor (page 6, paragraph [0084] and FIG. 5).

In re claim 14, as applied to claim 1 above, **Adan** discloses all claimed limitations including the limitation wherein the forming steps are according to a CMOS process (page 4, paragraph [0060]).

In re claim 15, as applied to claim 9 above, **Adan** discloses all claimed limitations including the limitation wherein first **C2** and second **Cf** gates are N-type gates (page 3, paragraph [0052]).

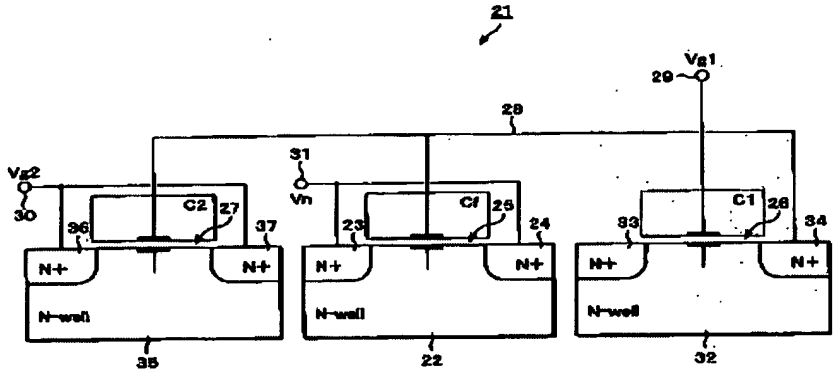
In re claim 18, as applied to claim 1 above, **Adan** discloses all claimed limitations including the limitation forming another differential varactor element on the semiconductor, the another differential varactor element comprising first, second and third P+ doped regions in a P well, a first gate for controlling the first and second P+ doped regions and a second gate for controlling said second and third P+ doped regions,

and connecting said first, second and third P+ doped regions to receive power from the voltage source (FIG. 5).

In re claim 31, **Adan** disclose a method of forming a semiconductor varactor device 21 having improved linearity comprising the steps of:

providing a semiconductor substrate (single silicon substrate) (page 4, paragraph [0055]); forming at least a first and a second differential varactor element on the semiconductor substrate, the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35,**

FIG. 5



forming a first gate **C2** for controlling the first **36** and second **37** N+ doped regions and forming a second gate **Cf** for controlling the second **37** and third **24** N+ doped regions (pages 3-4, paragraphs [0051]-[0053] and FIG. 5); forming a first and second resistor in the substrate connected in series and connected to receive power from a voltage source;

connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor element to receive power having a the first voltage **Vg2**; and

connecting the first **33**, second **34** and third N+ doped regions of the second differential varactor element to voltage source through the first resistor so as to receive power having a second voltage **Vg1**, different than the first voltage; and connecting the first, second, and third N+ doped regions of the third differential varactor element to the voltage source through both of the first and second resistors so as to receive power having a third voltage (page 4, paragraphs [0053]-[0055] and FIG. 5).

Adan disclose forming at least a first and a second differential varactor element on the semiconductor substrate wherein the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35** but does not explicitly discloses that the steps of forming first, second and third N+ doped regions in the same N well as recited in independent claim 31.

Yeo, however, discloses a method of forming a semiconductor varactor device comprising the steps of: providing a semiconductor substrate 96; forming a differential varactor element on the semiconductor substrate 96, the forming of the differential varactor elements comprising forming first, second and third N+ doped region 104 in the same N well 100 (col. 5, lines 59-65), forming a first gate 108 for controlling the first and second N+ doped regions 104 and forming a second gate for controlling the second and third N+ doped regions 104 (col. 6, lines 10-42 and FIG. 9).

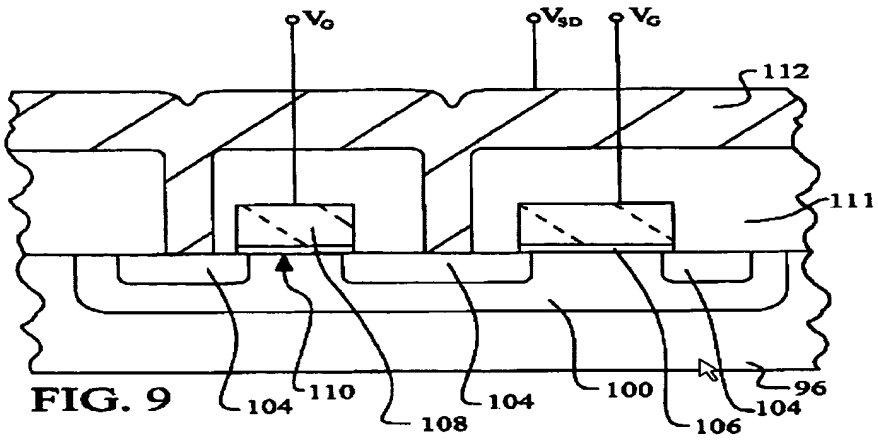


FIG. 9

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Yeo to enable the process of forming the first, second and third N+ doped regions in the same N well of Adan to be performed and furthermore to obtain a high performance varactor on silicon in the manufacture of integrated circuit devices (col. 1, lines 8-11, Yeo).

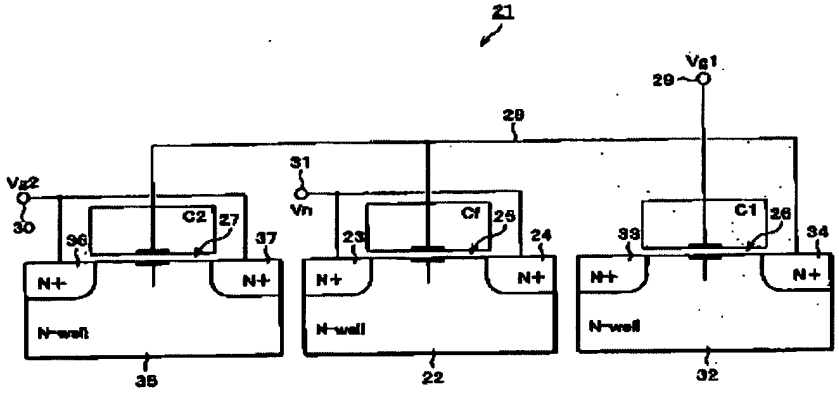
In re claim 33, as applied to claim 31 above, **Adan** discloses all claimed limitations including the limitation wherein the method further comprising the steps of connecting the first gate of the first, second and third differential varactor elements together at a first terminal and connecting the second gate of the first, second and third differential varactor element together at a second terminal (FIG. 5).

In re claim 34, as applied to claim 31 above, **Adan** discloses all claimed limitations including the limitation wherein the first and second gates are N-type gates (page 3, paragraphs [0051] and [0052]).

In re claim 35, **Adan** disclose a method of forming a semiconductor varactor device 21 having improved linearity comprising the steps of:

providing a semiconductor substrate (single silicon substrate) (page 4, paragraph [0055]); forming at least a plurality of differential varactor element on the semiconductor substrate, the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35,**

FIG. 5



forming a first gate **C2** for controlling the first **36** and second **37** N+ doped regions and forming a second gate **Cf** for controlling the second **37** and third **24** N+ doped regions (pages 3-4, paragraphs [0051]-[0053] and FIG. 5); forming a plurality of resistors connected to to receive power from a voltage source and connected in series such that nodes are defined between adjacent ones of the serially connected plurality of resistors; and

connecting the first **36**, second **37** and third **24** N+ doped regions of the plurality of differential varactor elements to one each of the nodes such the first **33**, second **34** and third N+ doped regions of different ones of the plurality of differential varactor element are electrically separated by one of the plurality of (page 4, paragraphs [0053]-[0055] and FIG. 5).

Adan disclose forming at least a first and a second differential varactor element on the semiconductor substrate wherein the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35** but does not explicitly discloses that the steps of forming first, second and third N+ doped regions in the same N well as recited in independent claim 31.

Yeo, however, discloses a method of forming a semiconductor varactor device comprising the steps of: providing a semiconductor substrate 96; forming a differential varactor element on the semiconductor substrate 96, the forming of the differential varactor elements comprising forming first, second and third N+ doped region 104 in the same N well 100 (col. 5, lines 59-65), forming a first gate 108 for controlling the first and second N+ doped regions 104 and forming a second gate for controlling the second and third N+ doped regions 104 (col. 6, lines 10-42 and FIG. 9).

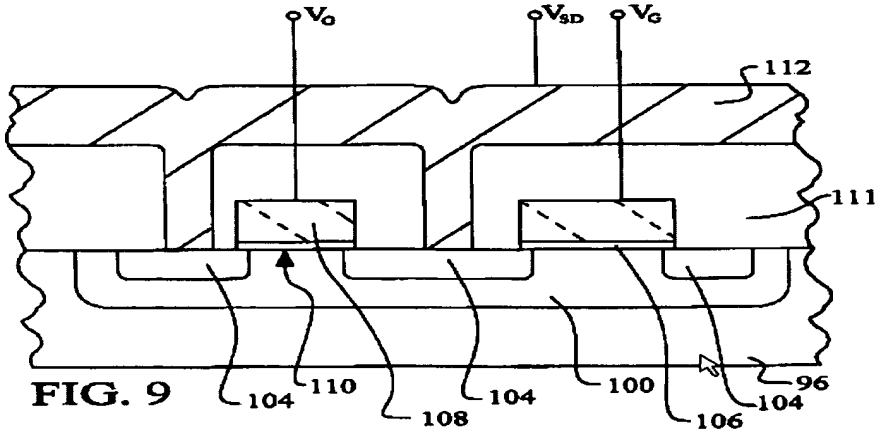


FIG. 9

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Yeo to enable the process of forming the first, second and third N+ doped regions in the same N well of

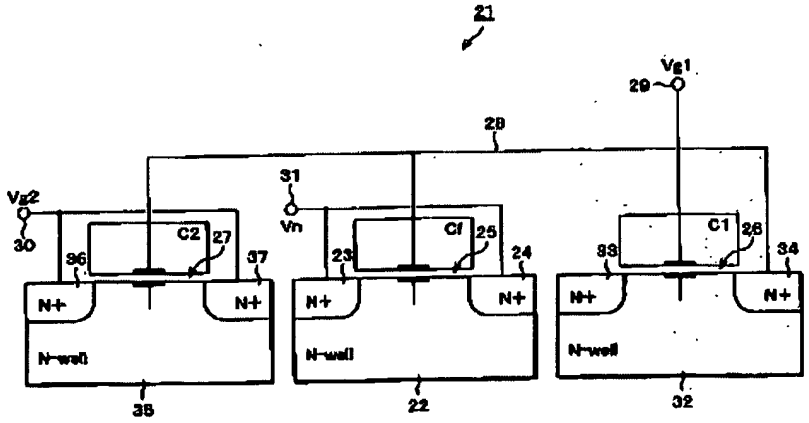
Adan to be performed and furthermore to obtain a high performance varactor on silicon in the manufacture of integrated circuit devices (col. 1, lines 8-11, Yeo).

In re claim 37, as applied to claim 35 above, **Adan** discloses all claimed limitations including the limitation wherein the method further comprising the steps of connecting the plurality of differential varactor elements together at a first terminal and connecting the second gate of the plurality of differential varactor element together at a second terminal (FIG. 5).

In re claim 40, **Adan** disclose a method of forming a semiconductor varactor device 21 having improved linearity comprising the steps of:

providing a semiconductor substrate (single silicon substrate) (page 4, paragraph [0055]); forming at least a first and a second, and third differential varactor element on the semiconductor substrate, the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35,**

FIG. 5



forming a first gate **C2** for controlling the first **36** and second **37** N+ doped regions and forming a second gate **Cf** for controlling the second **37** and third **24** N+ doped regions (pages 3-4, paragraphs [0051]-[0053] and FIG. 5);

connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor element to receive power having a the same first voltage **Vg2**; and connecting the first **33**, second **34** and third N+ doped regions of the second differential varactor element together so as to receive power having the same second voltage **Vg1**, the second voltage being different than the first voltage (page 4, paragraphs [0053]-[0055] and FIG. 5);

connecting the first **36**, second **37** and third **24** N+ doped regions of the third differential varactor element to receive power having a the same third voltage **Vg2**; the third voltage being different than the first and second voltage (page 4, paragraphs [0053]-[0055] and FIG. 5).

Adan disclose forming at least a first and a second differential varactor element on the semiconductor substrate wherein the forming of each of the differential varactor elements comprising the steps of forming first **36**, second **37** and third **24** N+ doped regions the N well **22, 32, 35** but does not explicitly discloses that the steps of forming first, second and third N+ doped regions in the same N well as recited in independent claim 1.

Yeo, however, discloses a method of forming a semiconductor varactor device comprising the steps of: providing a semiconductor substrate 96; forming a differential varactor element on the semiconductor substrate 96, the forming of the differential

varactor elements comprising forming first, second and third N+ doped region 104 in the same N well 100 (col. 5, lines 59-65), forming a first gate 108 for controlling the first and second N+ doped regions 104 and forming a second gate for controlling the second and third N+ doped regions 104 (col. 6, lines 10-42 and FIG. 9).

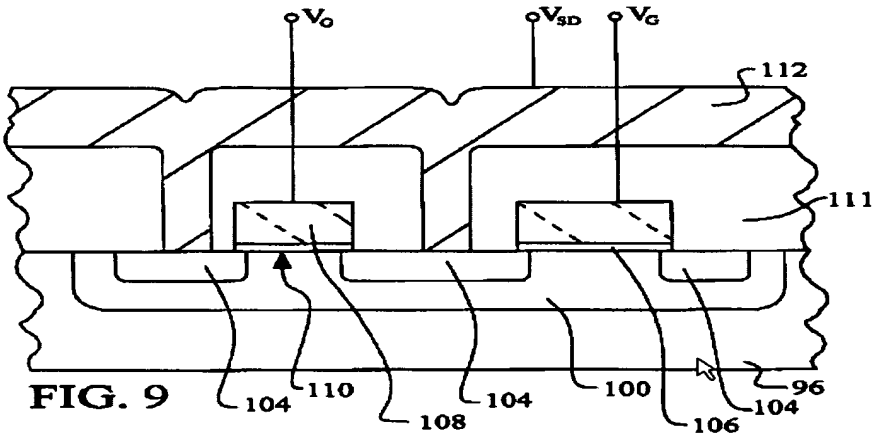


FIG. 9

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Yeo to enable the process of forming the first, second and third N+ doped regions in the same N well of Adan to be performed and furthermore to obtain a high performance varactor on silicon in the manufacture of integrated circuit devices (col. 1, lines 8-11, Yeo).

3. Claims 2, 4, 19, 32 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adan (U.S. Pub. 2003/0136992) in view of Yeo et al. (U.S. Patent 6,521,939) as applied to claims 1, 31, and 35 above, and further in view of Jasa et al. (U.S. Pub. 2005/0212609).

In re claim 2, as applied to claim 1 Paragraph 2 above, **Adan** discloses all claimed limitations including the limitation wherein the step of connecting the first **36**, second **37**

and third **24** N+ doped regions of the first differential varactor comprises connecting to the voltage source **Vg2** (FIG. 5) but does not explicitly discloses wherein the step of connecting the first, second and third N+ doped regions of the second differential varactor comprises connecting the region to the voltage source and to the first terminal of the first resistor so that power from the voltage source received at the differential varactor passes through the first resistor resulting in a voltage drop.

Jasa, however, discloses a varactor pair having the step of connecting the first, second and third N+ doped regions of the common N Well of the second differential varactor comprises connecting the regions to the voltage source V_{cp} and to the first terminal of the first resistor so that power from the voltage source at the differential varactor passes through the first resistor **R3** resulting in a voltage drop (page 3, paragraphs [0028]-[0030] and FIG. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Jasa to enable the process of connecting the first, second and third N+ doped regions of the second differential varactor comprises connecting to the voltage source through the first resistor of Adan to be performed and furthermore to generate a differential oscillating waveform (col. 2, paragraph [0012], Jasa).

In re claim 4, as applied to claim 2 above, **Adan** discloses all claimed limitations including the limitation wherein the step of connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor comprises connecting to the voltage source **Vg2** (FIG. 5) but does not explicitly disclose connecting the regions to the voltage

source through another resistor, and such that the second differential varactor elements receive power from the voltage source through both of another and the first resistors.

Jasa, however, discloses a varactor pair having the step of connecting the first, second and third N+ doped regions of the common N Well of the second differential varactor comprises connecting to the voltage source V_{cn} through the another resistor **R2**, and such that the second differential varactor elements received power from the voltage source V_{cn} through both of another **R2** and the first **R1** resistors (page 3, paragraphs [0028]-[0030] and FIG. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Jasa to enable the process of connecting the regions to the voltage source through another resistor, and such that the second differential varactor elements receive power from the voltage source through both of another and the first resistors to be performed and furthermore to generate a differential oscillating waveform (col. 2, paragraph [0012], Jasa).

In re claim 19, as applied to claim 2 above, neither Adan nor Jasa disclsoes that the step of forming the first resistor from a polysilicon material. The reference, Ohkubo et al. (U.S. Pub. 2004/0188795), provided herein as evidence to show that the process of forming the first resistor from a polysilicon material is well-known to one of ordinary skill in the art at the time of the invention was made (page 2, paragraph [0015], Ohkubo).

In re claim 32, as applied to claim 2 above, **Adan** discloses all claimed limitations including the limitation wherein the step of connecting the first **36**, second **37** and third **24** N+ doped regions of the first differential varactor comprises connecting to the voltage

source **Vg2** (FIG. 5) but does not explicitly disclose connecting the regions to the voltage source through another resistor, and such that the second differential varactor elements receive power from the voltage source through both of another and the first resistors.

Jasa, however, discloses a varactor pair having the step of connecting the first, second and third N+ doped regions of the common N Well of the second differential varactor comprises connecting to the voltage source V_{cn} through the another resistor **R2**, and such that the second differential varactor elements received power from the voltage source V_{cn} through both of another **R2** and the first **R1** resistors (page 3, paragraphs [0028]-[0030] and FIG. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan and Jasa to enable the process of connecting the regions to the voltage source through another resistor, and such that the second differential varactor elements receive power from the voltage source through both of another and the first resistors to be performed and furthermore to generate a differential oscillating waveform (col. 2, paragraph [0012], Jasa).

In re claim 36, neither **Adan** nor **Yeo** teach or suggest that the step of forming a plurality of resistors further comprises the step of forming a plurality of resistors and another resistor and connecting another resistor in series between the voltage source and the serially connected plurality of resistor.

Jasa, however, discloses a the step of forming a plurality of resistors further comprises the step of forming a plurality of resistors and another resistor and connecting

another resistor in series between the voltage source and the serially connected plurality of resistor (page 3, paragraphs [0028]-[0030] and FIG. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Adan, Yeo and Jasa to generate a differential oscillating waveform (col. 2, paragraph [0012], Jasa).

Allowable Subject Matter

4. Claims 5-8, 10, 11, 13, 16, 17, 38 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Applicant's Amendment and Arguments

5. Applicant's arguments with respect to claim 1-19 and 31-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
September 02, 2006

Brook Kebede
BROOK KEBEDE
PRIMARY EXAMINER